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EXAMINER
THOMAS, SHANE M

ART UNIT	PAPER NUMBER
2186	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/079,097	YOO ET AL.	
	Examiner	Art Unit	
	Shane M Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-51 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-51 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 February 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The abstract of the disclosure is objected to for the following:

(i) page 9, the applicant refers to RCLK as both the read clock (lines 7 and 17) and return clock (line 23);

(ii) page 10, line 9, and page 14, line 16 there exists superfluous periods;

(iii) page 31, line 14 should be removed from the abstract.

Correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-44,49, and 51 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1,12,23,34,41, line 1, it is not clear whether the --memory module-- or --memory system-- comprise the limitations of claims 1,12 respectively. Further, it is not clear if the --first memory module-- of line 2 is the --memory module-- for use in the memory system of line 1. As such, the examiner is interpreting both --first memory module-- and -second memory module-- of line 13 to be identical memory modules, both of which are used in a memory

system, the memory system comprising the limitations of claim 1. Further regarding claim 1, the placement of the --second buffer-- is indefinite and open to multiple interpretations; one interpretation is that the --second buffer-- could either be contained in the first memory module or as an outside element in the memory system. For the purposes of examination, the examiner will regard the --second buffer-- to be contained in the first memory module.

As per claim 4, it is not clear whether the term --the memory-- of line 3 refers to the memory module or the memory device contained within the memory module as --the memory-- lacks antecedent basis. The examiner will examine claim 4 with regard to --the memory-- being the memory device of the first memory device as described in claim 1.

As per claim 6, it is unclear whether the term --the data signals-- refers to the set of signals that data is transferred on to and from the second buffer or if --the data signals-- include every signal connected to the second buffer as --the data signals-- lack antecedent basis. The examiner will regard --the data signals-- as the signals used to transfer data to and from the memory device. Further it is not clear whether the term --the memory-- refers to the --memory device-- or the --memory module-- as --the memory-- lacks antecedent basis. The examiner will regard --the memory-- as the --memory device--.

As per claim 7, it is unclear whether the first memory module and second memory module are identical designs; therefore the term --the second buffer-- (line 3) contained in the second memory module lacks antecedent basis. For the purposes of examination, the examiner will examine the claim with regard to the first and second memory modules being identical designs, and the second memory module comprising a --second buffer--.

As per claims 10 and 32, it is not clear whether the term --buffered first latency signal-- of line 2 refers to the term --first latency signal-- or another signal as --buffered first latency signal-- lacks antecedent basis. For the purposes of examination, the examiner will examine the claim with regard to the --buffered first latency signal-- as being the --first latency signal-- that is buffered by the first buffer.

As per claim 14, it is not clear whether the term -- the first module-- (line 4) refers to the first memory module or another module as --first module-- lacks antecedent basis. For the purposes of examination, the examiner will examine the claim with regard to --the first module-- as referring to the --first memory module--.

As per claim 19, the same rejection as claim 7 applies. It is not clear whether the first and second memory modules have identical designs; therefore, it is not clear whether the second module comprises a memory device. Thus --the memory device-- lacks antecedent basis. The examiner will regard the second memory module as being of identical design as the first memory module.

As per claims 32 and 33, it is not clear whether the term --the first buffer-- (line 1) refers to --the buffer-- of claim 23 or another buffer as the --the first buffer-- lacks antecedent basis. A --first-- and --second-- buffer are defined in claim 31. The examiner will regard --the first buffer-- as the --first buffer-- of claim 31.

As per claim 33, it is unclear whether the term --the first latency signal-- refers to the --first latency signal-- of claim 32 or a different signal as --the first latency signal lacks antecedent basis. For the purposes of examination, the examiner will regard the --first latency signal-- as being defined in claim 32.

As per claim 38, the same rejection as claims 7 and 19 apply regarding --the memory device on the second memory module-- (line 5). The examiner will regard the second memory module as being of identical design as the first memory module.

As per claim 42, only a --first memory module-- has been defined thus far (claim 41); therefore, the term --the second memory module-- lacks antecedent basis. The examiner will examiner the claim with regard to the memory system of claim 41 comprising a second memory module of identical design as the first memory module.

As per claim 49, it is unclear whether the term --the first module-- of line 9 refers to the first memory module of line 2 or another module as --the first module-- lacks antecedent basis. The examiner will examiner the claim with regard to --the first module-- as referring to the --first memory module--.

As per claim 51, line 2 is indefinite in that the line could be interpreted to read that the --first write clock signal-- is being received at a buffer on an first memory module *and* also being received at a memory device or that the --first write clock signal-- is being received at a buffer on a first memory module and that memory module includes a memory device. Clarification is required.

Claims 2,3,5,8,9,11,13,15-18,20-22,24-31,35-37,39,40,43, and 44 are rejected since they carry the same limitations as rejected claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

It seems that two typographical errors have been made: one on lines 27 and 33 of column 6 and another on line 9 of column 5.

Regarding column 6, lines 27 and 33, whereas both lines read "memory bus 550," it is apparent to the examiner that the lines should read "memory bus 570." This correction is supported by the fact that lines 11-25 discuss memory bus 550 and its constitution (memory-data lines, address lines, control lines, etc) whereas lines 26-42 begin to discuss memory bus 570 (line 26) and then repeat the information regarding memory bus 550 that was stated above in lines 11-25. To further support this error, lines 26-42 do not mention the ability of bus 570 to receive data from the buffer 500, whereas column 4, lines 54-62, states that bus 330 can transmit and receive data. Figure 5 shows a block-level diagram of one of the memory modules of figure 4; therefore, it can be seen that the bus 330 corresponds to bus 570. Nonetheless, the examiner shall regard element number 550 in column 6, lines 27 and 33, as element number 570.

Regarding column 5, line 9, whereas the line reads "bus 325," it is apparent to the examiner that the line should read, "bus 320." The correction is supported by the fact that lines 5-8 of column 5, discuss data transmission from bus 320 to bus 325 of figure 4, and that data can also be transmitted from memory module 310b to memory module 310a via bus 325 (refer to

lines 17-20 of column 6). Further, the language of column 5, lines 8-10, is inconsistent. These lines describe data transmission from buffer 312b to buffer 312a and the data being "routed through" port 315a to bus 325. However, bus 325 is the originating bus the data is being routed *from*. Nonetheless, the examiner shall regard bus 325 in column 5, line 9, as being bus 320.

As per claim 23, lines 1-6, and claim 49, lines 1-6, Halbert shows a first memory module 310a in figure 4 that includes a memory device 311a and a buffer 312a. Buses 320 and 325 connected to the first memory module correspond to buses 550 and 570 respectively, of figure 5. Address lines, command lines, and clock signals (from here on out referred to as ADD/CMD lines) as well as memory-data can be sent and received along both buses (column 6, lines 11-42). From here on out, the examiner will refer to the combination of memory-data and ADD/CMD lines as --data lines--. The examiner will refer to a --first direction of transmission-- as the flow of signals on data lines being transmitted to the buffer 500 from bus 550 and being received by the bus 570 to flow to other memory modules or a memory controller. In other words the first direction of transmission is a "left-to-right" or "clockwise" propagation of data through the memory system shown in figure 4. Likewise, the examiner will refer to a --second direction of transmission-- as the flow of signals on data lines being transmitted to the buffer 500 from bus 570 and being received by the bus 550 to flow to other memory modules or a memory controller. The second direction can be equated to a "right-to-left" or "counter-clockwise" propagation of data through the memory system of figure 4. These directions of data flow are further described in column 6, lines 11-42.

The examiner is regarding the clock signal of the ADD/CMD lines that is input into the buffer 500 from bus 550 (first direction of transmission) as a --first write clock signal--, and the command lines of the ADD/CMD lines to be control lines carrying a read, write, etc. command since data can be read and written to memory modules 560 (column 8, lines 34-35). The examiner is also regarding the clock signal portion of the ADD/CMD lines being transferred in the second direction of transmission as a --first read clock signal--.

Regarding lines 7-9 of claim 23 and lines 7-9 of claim 49, the clock signal of the ADD/CMD lines that is sent to the memory devices 560 from the buffer 500 via bus 560i will be regarded as a --memory write clock signal--. As was discussed above, the --first write clock signal-- is received by the buffer via bus 550 (in the first direction of transmission). After this reception, the buffer 500 then generates the --memory write clock signal-- and outputs it to the memory devices (along with the command lines indicating a write command) via bus 560i (refer to column 8, lines 34-37).

As per claims 24,35 and 42, data lines (ADD/CMD and memory-data) are received at port 501a from bus 550 as discussed above. The ADD/CMD lines include the first write clock signal as discussed above as well. Because memory-data can be transferred from one memory module to another via bus 570 (column 6, lines 26-42), the examiner is considering the clock signal generated by the buffer 500 as a result of the data lines being routed from port 501a (column 5, lines 5-8) to be a --second write clock signal--. As previously discussed, the command lines control data transmission and data lines can be transmitted from memory module to memory module; therefore, it is inherent that there be some control of which memory module's memory device in which to write data. Thus if memory-data is routed from one

memory module to another, the command lines are controlling the writing of data when data is written to the memory devices. As can be seen in figures 4 and 5, all data lines are routed through the buffer 500 of each memory module.

As per claims 26 and 44, the examiner is considering the --first write clock signal-- portion of the ADD/CMD lines (input into the buffer 500 via bus 550) output (from the buffer) to the memory devices 560 via bus 560i to be a --memory write clock signal--. As is know in the art, if the command lines of the ADD/CMD lines contain a memory read for the memory devices, the address lines of the ADD/CMD lines are input into the memory device to access data (refer to column 8, lines 34-37). Once valid data exists on buses 560a-560i, the examiner is considering the clocking signal used to clock the data from the memory devices 560 into the buffer 500 to be a --memory read data clock signal--.

As per claims 30 and 37, the examiner is now referring to memory module 310b as the --first memory module-- and memory module 310a as the --second memory module--. Since data can be transmitted from the buffer 500 via bus 550 of one memory module to bus 570 of another memory module (column 6, lines 20-23), the examiner will regard the clock signal of the ADD/CMD lines sent from the buffer 500 of memory module 310b to be a --second read clock signal--. Because data lines are sent from bus 550, the data is going in the second direction of transmission. As discussed above in claim 23's rejection, the --first write clock signal-- is received from bus 550 at the buffer (in this case, buffer 312b) along with the other ADD/CMD lines. These command lines control data transmission and data lines can be transmitted from memory module to memory module; therefore, it is inherent that there be some control to read data from the memory module's memory device so data can ultimately be retrieved from the

memory system. Because of the point-to-point connection between the memory modules, when a command to read data is issued, that read data must be transferred from memory module to memory module until the data reaches it's target destination (usually the memory controller - refer to column 6, lines 11-25). Thus, when such a command is issued to a first memory module, data can be transmitted (read from the first memory module) to a second memory module.

As per claim 34, the rejection for lines 1-6 follows the rejection for lines 1-6 of claim 23. The rejection for lines 7-11 follows the rejection of claim 26.

As per claim 36 and 43, the rejection follows the rejection for lines 7-9 of claim 23.

As per claim 41, the rejection for lines 1-6 follows the rejection for lines 1-6 of claim 23. The rejection for lines 7-10 follows the rejection for claims 30 and 37.

As per claim 45, Halbert shows a memory controller 111 in figure 4 which generates the data signals (ADD/CMD lines and memory-data lines) between the processor 101 and the memory system 113 (which is comprised of memory modules 310a and 310b in figure 4) (refer to column 3, lines 25-30). The examiner is regarding the clock signal (part of the ADD/CMD lines) that the memory controller generates as a --first write clock signal--, and as discussed above, the command lines transmit read and write commands. The rejection of lines 4-7 of claim 45 follows the rejection for lines 2-6 of claim 23. The rejection of lines 8-11 of claim 45 follows the rejection for claims 24,35 and 42. The rejection of lines 11 (starting at "and generating...") - 14 of claim 45 follows the rejection of claim 26. Finally, the rejection of lines 15-18 of claim 45 follows the rejection for lines 7-9 of claim 23.

As per claim 46, the examiner is considering the processor 101 of the memory system of figure 1 to be a --read clock generator-- since, as is known in the art, a processor can issue a read

command to read instructions stored in a memory system 113 (column 3, lines 15-17). When a read command is issued, the examiner is considering the clock signal used to read data from the memory devices as a --read clock signal--. Thus the --first read clock signal-- (input into a first memory module in the first direction of transmission), or a signal used to begin the read process, is generated as a result of the processor request. Lines 1-3 and 5-19 follow the rejection for claim 45. The rejection of lines 20-22 follows the rejection of claims 30 and 37.

As per claim 50, the rejection for lines 1-7 follows the rejection for claims 23 and 49. The rejection of lines 8-11 follows the rejection of claim 26.

As per claim 51, the rejection for lines 1-6 follows the rejection for lines 1-6 of claims 23 and 49. The rejection of lines 7-10 follows the rejection of claims 30 and 37.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4,6,7,9-15,18-21,27,31-33,38-40,47, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert et al. (U.S. Patent No. 6,625,687) in view of Gustavson (U.S. Patent No. 6,442,644).

As per claims 1 and 47, Halbert, as discussed above, shows a first memory module 312a and memory device 311a in figure 4 and states in column 8, lines 33-42, that two physically processing circuits ("buffers" - column 4, lines 63-64) are conceived in a preferred embodiment: both a buffer for the ADD/CMD lines and a buffer for the memory-data connected to the memory devices. However, Halbert does not depict the interaction or connection between the two buffers. Gustavson shows a diagram of a memory system in figure 3 that contains command-side buffer 301 and data-side buffer 302. Further, Gustavson shows the connection between the two buffers and a memory device, SLDRAMs. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the dual buffer design of the memory system of Gustavson with the memory system of Halbert since Halbert suggested that a dual buffer system could have been used, which would have effectively enabled a more straightforward data line topology than a unitary system (Halbert, column 8, lines 39-42). Further, Halbert states that any memory devices (311a and 311b of Halbert figure 4) can be used in the memory system. Therefore it would have been obvious to one having ordinary skill in the art to have used the SLDRAMs memory devices of Gustavson since the SLDRAMs are capable of being adjusted or calibrated (column 4, lines 53-55, of Gustavson) and since they are a form of DRAM module such as the other examples of possible memory devices used by Halbert (column 2, lines 65-67 of Halbert). The examiner is using the Gustavson reference to demonstrate how the signals of buffer 500 of Halbert could have been used had buffer 500 been comprised of dual buffers - one for ADD/CMD lines and one for memory-data lines (column 8, lines 34-42).

The command-side buffer (--first buffer--) 301 buffers the CCLK, data and command/address data (refer to figure 1 of Gustavson), and the data-side buffer (--second buffer--) 302 buffers data to and from the memory devices and the DCLK and memory-data bus DQ (figure 3 of Gustavson). For the purposes of clarification, figure 3 shows the CommandLink bus 351 and DataLinks buses whose signals are defined in figure 1. The examiner is considering that the ADD/CMD and memory-data signals of Halbert could have been the CommandLink and DataLink signals of Gustavson, respectively. The --first write clock signal-- could have been sent to both command-side and data-side buses via clock lines CCLK and DCLK, respectively (column 30, lines 20-26). The examiner is also considering the --first read clock signal-- sent to buffer of Halbert in the second direction of transmission to have been sent to the data-side buffer as described in column 10, lines 10-20 of Gustavson. A first memory module would have sent a DCLK, or --first read clock signal--, to another module and then waited for the response of the data from the other memory module as suggested in column 10, lines 10-20.

Regarding lines 7-10 of claim 1, the rejection follows the rejection of claim 24 above in the 35 U.S.C. §102 rejections. The data-side buffer 302 (second buffer) of Gustavson would have contained the memory-data read and written to the buffer of 312a of Halbert. Therefore, when memory-data would have been routed through memory module 310a to 310b (Halbert, column 5, lines 5-8), it would have passed through the data-side buffer.

Regarding lines 10 (starting at "and generating...") - 13 of claim 1, the rejection follows the rejection for lines 7-9 of claim 23 above in the 35 U.S.C. § 102 rejections. The data-side buffer 302 would have contained the memory-data that was written to and read from the memory devices (i.e. SLDRAMs).

Regarding lines 14-18 of claim 1, the rejection follows the rejection for lines 7-11 of claim 34 above in the 35 U.S.C. § 102 rejections.

As per claims 2 and 18, the rejection follows the rejection for claim 30 above.

As per claims 3,15, and 27, the examiner is considering the --memory read clock signal-- to be the DCLK signal returned from the SLDRAM memory device when data was being read out as discussed in column 26, lines 42-48. As was previously discussed in claim 34's rejection of lines 7-11, the --memory write data clock-- would have been the clock signal sent to the memory devices.

As per claim 4, as can be seen in figure 5 of Halbert, the transmission path of the --memory write clock signal-- (bus 560i) would have been coupled to the transmission path of --memory read clock signal-- (buses 560a - 560h) of the buffer 500 (which the examiner is considering to be the data-side buffer in this case). The --memory write clock signal-- and --memory read clock signal-- would have been sent and received from and to port 502, respectively.

As per claim 6, the examiner is considering the transmission path of the data signals (560a-560h) between the buffer 500 of Halbert (--second buffer-- in this case) and the memory devices to be --substantially equal-- to the lengths of the transmission paths of the --memory write clock signal-- (560i) and --memory read clock signal-- (DCLK, which is part of 560a-560h). Additionally it could have been seen that these three transmissions paths are --substantially equal-- in length using figure 3 of Gustavson. --Memory write clock signal--, --memory read clock signal--, and the data signals between the memory devices and the data-side

buffer 302 (--second buffer--) are all transferred via the bus between the data-side buffer and the SLDRAM memory devices; thus, they are all --substantially equal-- in length.

As per claim 7, and regarding the discussion above in claim 24's rejection, a --first write clock signal-- would have been input into the data-side buffer 302 (--second buffer--) and a --second write clock signal-- would have been generated and sent to a second memory module. Further, the examiner is considering the --second write clock signal-- that would have been output from the first memory module, to be the --first write clock signal-- of the second memory module. Since the --first write clock signal-- would have been input into the data-side buffer 302 of a memory module, as discussed in claim 1's rejection, therefore, the --second write clock signal-- of a first memory module (310a of figure 4 Halbert for example) would have been input into the data-side buffer 302 (--second buffer--) of a second memory module (310b of figure 4 for example).

As per claims 8,22, and 25, Gustavson shows a delay locked loop (DLL) 720 comprised inside the SLDRAM module 750 in figure 7. As discussed above, the examiner is considering the –first write clock signal—as being a portion of the ADD/CMD lines than enters a memory module. The CCLK clock 708 is the –first write clock signal--, and the DCLK signal is the –second write clock signal—also discussed above. Thus, as could have been seen in figure 7, the --second write clock signal— could have been generated by a delay locked loop (DLL) 720.

As per claims 9,19,31 and 38, since data could have been written and read and transmitted in both direction of the memory system in figure 4 of Halbert as discussed in claim 23's rejection above, it is inherent that a [decoded] signal could have been sent to the --second buffer-- of a given memory module because data must either be routed from another module

(column 5, lines 5-10, of Halbert) or accessing the memory device of the current module and then routed to the requesting apparatus. Therefore there would have been a signal from the ADD/CMD lines that would have controlled the memory modules to have either accessed the memory modules' memory devices or routed the data to another memory module. As discussed in the rejection of claim 1, the ADD/CMD lines would have been input into the command-side buffer (--first buffer--).

As per claims 10,20,32 and 39, in one embodiment of the memory system of Halbert, the buffer 500 (in this case the command-line buffer or --first buffer--) would have synchronized data (part of which are the ADD/CMD lines that are input into the first buffer) from buses 550 and 570 at the data synchronization circuit module 520 (column 7, lines 3-7). The examiner is considering the bus that could have carried the later arriving data as a --first latency signal--. The write or read transaction clock signal (--first write clock signal--) would have accompanied the ADD/CMD lines sent on the bus (column 6, lines11-16) as previously discussed. Once the data was synchronized for the data operation, the synchronized data or --buffered first latency signal-- (since it leaves the first buffer) would have been sent to the memory device (column 7, lines 14-20).

As per claims 11,21,33, and 40, the examiner is regarding the --buffered first latency signal-- that would have been output from the first buffer as a --second latency signal-- since the first buffer would have manipulated the --first latency signal-- (synchronized the signal with another bus' data) and then outputted a new, different --latency-- signal (which would have then been synchronized); hence, a --second latency signal--.

As per claim 12, the rejection follows the rejection for lines 1-10 of claim.

As per claim 13, the rejection follows the rejection for lines 10 (beginning with "and generating") - 13 of claim 1.

As per claim 14, the rejection follows the rejection for lines 14-18 of claim 1.

As per claims 17 and 29, as previously discussed in claim 3's (and 34's) rejection, when a memory read takes place, the examiner is considering the clock signal that would have been returned from the memory device as a result of the input –memory write clock signal—to be the –memory read clock signal--. As could have been seen in figure 7 of Gustavson, the delay locked loop 720 would have been coupled to the transmission path of the – memory read clock signal—(DCLK) and the –memory write clock signal—(CCLK).

As per claim 48, the rejection follows the rejection for lines 1-10 of claim 1.

Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert et al. (U.S. Patent No. 6,625,687) in view of Gustavson et al. (U.S. Patent No. 6,442,644) in further view of Johnson et al. (U.S. Patent No. 5,987,576).

As per claims 5 and 16, Halbert in view of Gustavson does not specifically show a memory system that utilizes dummy loads on the memory modules. Johnson et al. (U.S. Patent No. 5,987,576) teaches that --dummy loads-- are often implemented on memory modules to ensure that the electrical characteristics of the second clock segment track the electrical characteristics of the data bus as memory modules are inserted and removed (column 3, lines 57-60). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of dummy loads in the memory system of modified Halbert in order to have ensured that the memory system did not sacrifice performance issues when memory modules were inserted and removed (column 10, lines 38-

42). As can be seen in figure 4 of Johnson, the dummy loads are interposed on the memory modules; therefore, the dummy loads would have been interposed between the transmission paths between the --memory write clock signal-- and --memory read clock signal--. In other words, the dummy loads would have been connected in lieu of some or all of the memory devices 560 in figure 5 of Halbert.

Claim 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert et al. (U.S. Patent No. 6,625,687) in view of Johnson et al. (U.S. Patent No. 5,987,576). The rejection and motivation for combining Halbert and Johnson follows the rejection for claims 5 and 16 discussed above.

Conclusion

Prior art made of record and not relied upon and considered pertinent to applicant's disclosure are listed in PTO-892.

Wakerly (U.S. Patent No. 5,586,299) teaches transferring data from one memory module to another in figure 1.

Dodd et al. (U.S. Patent NO. 6,530,006) teaches a memory modules 120 using 2 buffers.

Osaka et al. (U.S. Patent Application Publication US2003/0007379) teaches a point-to-point memory module organization.

Leddige et al. (U.S. Patent No. 6,477,614) teaches a point-to-point interface of memory modules

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (703) 605-0725. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 764-7239 for regular communications and (703) 764-7239 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Shane M. Thomas

October 31, 2003

MATTHEW KIM
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